CLAIMS

1. An integrated circuit comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phases of the reference and feedback signals to determine a phase error between the reference and feedback signals, and provide a PFD output comprised of PFD values, wherein each PFD value is a multi-bit value determined by the phase error and a detector gain; and

a loop filter (LF) operative to receive and filter the PFD output and provide an LF output, wherein the LF output is updated for each PFD value received on the PFD output.

2. The integrated circuit of claim 1, further comprising:

an oscillator operative to receive the LF output and provide an oscillator signal having a phase determined by the LF output; and

a divider operative to receive the oscillator signal, divide the oscillator signal in frequency by a factor of N, where N is one or greater, and provide the feedback signal.

3. The integrated circuit of claim 1, wherein the detector gain is adjusted in an acquisition mode and maintained in a tracking mode.

4. The integrated circuit of claim 1, wherein the detector gain is initialized to a maximum value and thereafter decreased whenever a change in phase error polarity is detected.

5. The integrated circuit of claim 1, wherein the PFD is further operative to provide a clock signal having a pulse for each PFD value in the PFD output, and wherein the loop filter is operative to update the LF output with the clock signal.

6. The integrated circuit of claim 5, wherein the pulse in the clock signal for each PFD value is delayed by a particular amount of time relative to a start of the PFD value.

7. A device comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phases of the reference and feedback signals to determine a phase error between the reference and feedback signals, and provide a PFD output comprised of PFD values, wherein each PFD value is a multi-bit value determined by the phase error and a detector gain; and

a loop filter (LF) operative to receive and filter the PFD output and provide an LF output, wherein the LF output is updated for each PFD value received on the PFD output.

8. An apparatus comprising:

means for comparing phases of a reference signal and a feedback signal to determine a phase error between the reference and feedback signals;

means for providing a phase-frequency detector (PFD) output comprised of PFD values, wherein each PFD value is a multi-bit value determined by the phase error and a detector gain;

means for filtering the PFD output to obtain a loop filter (LF) output;

means for providing an oscillator signal having a phase determined by the LF output; and

means for dividing the oscillator signal in frequency by a factor of N to obtain the feedback signal, where N is one or greater.

9. An integrated circuit comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phase of the reference signal against phase of the feedback signal, and provide a detector output comprised of a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal; and

a loop filter (LF) operative to receive and filter the detector output and provide an LF output, wherein the loop filter is operative to adjust loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values.

10. The integrated circuit of claim 9, further comprising:

an oscillator operative to receive the LF output and provide an oscillator signal having a phase determined by the LF output; and

a divider operative to receive the oscillator signal, divide the oscillator signal in frequency by a factor of N, where N is one or greater, and provide the feedback signal.

11. The integrated circuit of claim 9, wherein the loop filter is operative to increase the loop bandwidth if a large phase error between the reference and feedback signals is detected.

12. The integrated circuit of claim 11, wherein the large phase error is detected if a particular number of consecutive phase error values with same polarity are received in the detector output.

13. The integrated circuit of claim 9, wherein the loop filter is operative to decrease the loop bandwidth if a small average phase error is detected.

14. The integrated circuit of claim 13, wherein the small average phase error is detected if, for a designated time window, the number of phase error values with a first polarity, indicating the phase of the reference signal being early, is equal to the number of phase error values with a second polarity, indicating the phase of the feedback signal being early.

15. A device comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phase of the reference signal against phase of the feedback signal, and provide a detector output comprised of a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal; and

a loop filter (LF) operative to receive and filter the detector output and provide an LF output, wherein the loop filter is operative to adjust loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values.

16. An apparatus comprising:

means for comparing phases of a reference signal and a feedback signal to determine a phase error between the reference and feedback signals;

means for providing a detector output comprised of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal;

means for filtering the detector output to obtain a loop filter (LF) output; and

means for adjusting loop bandwidth of a digital phase-locked loop (PLL) based on the sequence of phase error values.

17. An integrated circuit comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phases of the reference and feedback signals, and provide a PFD output;

a loop filter (LF) operative to receive and filter the PFD output and provide an LF output; and

a current digital-to-analog converter (iDAC) operative to receive and convert the LF output to current and provide an iDAC output, the iDAC including

a first section of L steered current sources, where L is an integer greater than one, each steered current source providing current to the iDAC output when switched on and to circuit ground when switched off, and

a second section of P single-ended current sources, where P is an integer one or greater, each single-ended current source providing current to the iDAC output when switched on.

18. The integrated circuit of claim 17, further comprising:

a current controlled oscillator (ICO) operative to receive the iDAC output and provide an oscillator signal having a phase determined by the iDAC output; and

a divider operative to receive the oscillator signal, divide frequency of the oscillator signal by a factor of N, where N is one or greater, and provide the feedback signal.

19. The integrated circuit of claim 17, wherein the P single-ended current sources are designed to provide same amounts of current.

20. The integrated circuit of claim 17, wherein the L steered current sources are designed to provide different amounts of current.

21. An integrated circuit comprising:

a phase-frequency detector (PFD) operative to receive a reference signal and a feedback signal, compare phases of the reference and feedback signals, and provide a detector output comprised of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal;

a scaling unit operative to receive and scale the detector output with a detector gain and provide a PFD output; and

a control unit operative to receive the detector output, detect for changes in polarity of the phase error values, and adjust the detector gain based on the detected changes in phase error polarity.

22. The integrated circuit of claim 21, wherein the PFD output comprises a sequence of PFD values, one PFD value for each phase error value in the detector output, each PFD value having a sign determined by the phase error value and a magnitude determined by the detector gain.

23. The integrated circuit of claim 21, wherein the control unit is operative to initialize the detector gain to a maximum value and thereafter decrease the detector gain whenever a change in phase error polarity is detected.

24. An apparatus comprising:

means for comparing phases of a reference signal and a feedback signal to determine a phase error between the reference and feedback signals;

means for providing a detector output comprised of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal;

means for scaling the detector output with a detector gain to obtain a phase-frequency detector (PFD) output;

means for detecting for changes in polarity of the phase error values; and

means for adjusting the detector gain based on detected changes in phase error polarity.

25. A method of performing phase-frequency detection (PFD), comprising:

comparing phases of a reference signal and a feedback signal to determine a phase error between the reference and feedback signals;

providing a detector output comprised of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal;

scaling the detector output with a detector gain to obtain a PFD output;

detecting for changes in polarity of the phase error values; and

adjusting the detector gain based on detected changes in phase error polarity.

26. An integrated circuit implementing a phase-frequency detector (PFD), comprising:

a first flip-flop operative to receive a reference signal and a reset signal and provide a first signal having transitions determined by the reference signal and being reset by the reset signal;

a second flip-flip operative to receive a feedback signal and the reset signal and provide a second signal having transitions determined by the feedback signal and being reset by the reset signal;

a first latch operative to receive an inverted first signal at a data input and the second signal at a clock input and provide a first output signal;

a second latch operative to receive an inverted second signal at a data input and the first signal at a clock input and provide a second output signal; and

reset circuitry operative to receive the first and second signals and provide the reset signal for the first and second flip-flops.

27. The integrated circuit of claim 26, wherein the first and second output signals indicate whether phase of the reference signal is early or late with respect to phase of the feedback signal.

28. The integrated circuit of claim 26, wherein the first and second output signals provide phase error values at a rate determined by frequencies of the reference and feedback signals.

29. The integrated circuit of claim 28, wherein one phase error value is provided for each phase comparison period, and wherein the reset signal resets the first and second flip-flops at the start of each phase comparison period.

30. An integrated circuit comprising:

a loop filter (LF) operative to receive and filter an LF input with first and second gains and provide an LF output; and

a control unit operative to receive a detector output from a phase-frequency detector (PFD) indicating whether phase of a reference signal is early or late with respect to phase of a feedback signal, perform phase error analysis on the detector output, and adjust the first and second gains based on results of the phase error analysis, wherein the first and second gains determine loop bandwidth and damping of a digital phase locked loop (PLL) that includes the loop filter and the phase-frequency detector.

31. The integrated circuit of claim 30, wherein the detector output comprises a sequence of phase error values, each phase error value indicating whether the phase of the reference signal is early or late with respect to the phase of the feedback signal.

32. The integrated circuit of claim 31, wherein the control unit is operative to increase the first gain, the second gain, or both the first and second gains, if a large phase error is detected.

33. The integrated circuit of claim 32, wherein the control unit is operative to detect for the large phase error by counting number of consecutive phase error values

with same polarity and comparing the number of consecutive same polarity phase error values against a predetermined count value.

34. The integrated circuit of claim 31, wherein the control unit is operative decrease the first gain, the second gain, or both the first and second gains if a small average phase error is detected.

35. The integrated circuit of claim 34, wherein the control unit is operative to detect for the small average phase error by counting the number of phase error values with a first polarity and the number of phase error values with a second polarity within a designated time window, and wherein the small average phase error is declared if the number of phase error values with the first polarity is equal to the number of phase error values with the second polarity.

36. An apparatus comprising:

means for receiving a detector output from a phase-frequency detector (PFD) indicating whether phase of a reference signal is early or late with respect to phase of a feedback signal;

means for detecting for a large phase error in the detector output;

means for detecting for a small average phase error in the detector output;

means for increasing loop bandwidth of a phase locked loop (PLL) if the large phase error is detected; and

means for decreasing the loop bandwidth if the small average phase error is detected.

37. A method of adjusting loop bandwidth of a digital phase-locked loop (PLL), comprising:

receiving a detector output from a phase-frequency detector (PFD) indicating whether phase of a reference signal is early or late with respect to phase of a feedback signal;

detecting for a large phase error in the detector output;

detecting for a small average phase error in the detector output;

increasing the loop bandwidth if the large phase error is detected; and

decreasing the loop bandwidth if the small average phase error is detected.

38. An integrated circuit implementing a loop filter (LF) for a digital phase-locked loop (PLL), comprising:

a first carry lookahead adder (CLA) operative to receive and sum a loop filter input and a current accumulated value and provide an updated accumulated value;

a latch operative to receive and store the updated accumulated value from the first CLA and provide the current accumulated value;

a first unit operative to receive and scale the current accumulated value with a first gain value and provide a first intermediate value;

a second unit operative to receive and scale the loop filter input with a second gain value and provide a second intermediate value; and

a second CLA operative to receive and sum the first and second intermediate values and provide a loop filter output.

39. The integrated circuit of claim 38, wherein the first and second units are multipliers.

40. The integrated circuit of claim 38, wherein the first and second units are multiplexers.

41. An integrated circuit implementing a current digital-to-analog converter (iDAC), comprising:

a first section of L steered current sources, where L is an integer greater than one, each steered current source providing current to an iDAC output when switched on and to circuit ground when switched off; and

a second section of P single-ended current sources, where P is an integer one or greater, each single-ended current source providing current to the iDAC output when switched on, wherein the P single-ended current sources provide same amounts of current.

42. The integrated circuit of claim 41, wherein the L steered current sources provide different amounts of current.

43. The integrated circuit of claim 41, wherein the first section implements L least significant bits of the iDAC, and wherein the second section implements M most significant bits of the iDAC, where $P = 2^M - 1$.

44. The integrated circuit of claim 43, wherein for a value of V in an M-bit digital control for the second section, where $0 \leq V \leq 2^M - 1$, V single-ended current sources selected from among the P single-ended current sources are switched on.